REMARKS

Claims 1, 7, 13, 17 and 20 are amended herein. Claims 1-8 and 10-23 remain pending in the application.

Claims 13 and 16 over Persaud

In the Office Action, claims 13 and 16 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Persaud, UK Patent Application No. GB2074762 ("Persaud"). The Applicants respectfully traverse the rejection.

Claims 13 and 16 recite, *inter alia*, each of a first agent and a second agent accessing different portions of a shared external non-dedicated memory simultaneously.

Persaud appears to teach a system and method for accessing a common memory by a plurality of processors (Persaud, Abstract). A master processor can access its own memory or any of the slave memories (Persaid, Abstract). The master processor generates synchronizing signals which are applied over a backplane to each of the slave processors (Persaud, page 2, lines 45-47). Handshaking between the master and slave processors is used to control which processor obtains access to an entire particular slave's memory at any point in time (Persaud, page 2, lines 8-21). The master processor accesses memory that is dedicated to a slave processor since each processor/memory combination is contained on a common card (Persaud, page 1, lines 39-43).

Persaud teaches the entire slave's dedicated memory is accessed alternately by either the slave processor or the master processor. In addition, the common memory that is being accessed by the master and slave is dedicated memory associated with a specific slave. Persaud fails to teach each of a first agent and a second agent accessing different portions of a shared memory simultaneously, much less a first agent and a second agent accessing external non-dedicated, as claimed by claims 13 and 16.

Simultaneous access of portions of a common memory greatly improves the speed at which a system is able to access data. Although Persaud eliminates wait states between access by different processors through

synchronization, Persaud's processors still alternately access common memory that is dedicated to a particular processor. Much of a common memory remains un-accessed even during a memory access by either of Persaud's master processor or slave processor. Applicants' invention eliminates a large number of time a processor spends waiting for access to a common resource.

In addition, Persaud's dedicated memory limits future expandability of a system memory architecture by not providing a centralized memory system. Applicants' providing simultaneous access to common external non-dedicated memory retains expandability of the memory system while providing for the benefits of multiple access to a common resource without wait states.

Accordingly, for at least all the above reasons, claims 13 and 16 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 1-8, 10-12, 20-21 and 23 over Wu in view of Persaud

In the Office Action, claims 1-8, 10-12, 20-21 and 23 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu, U.S. Patent No. 5,659,715 ("Wu") in view of Persaud. The Applicants respectfully traverse the rejection.

Claims 1-8, 10-12, 20-21 and 23 recite, *inter alia*, access of either portions or partitions of an external non-dedicated memory through a clock representation of a first agent's clock signal.

Wu appears to teach a first and second processor having access to a common memory bank (Fig. 3, items 302, 400 and 304 respectively). Address and data lines (Wu, items 306 and 308) running to the common memory bank (Wu, item 304) are routed through a single source, the graphics controller (Wu, item 400). The CPU (item 302) and the graphics controller are tied together to route data to the common memory (Wu, Fig. 3). The common memory is connected with to the graphics controller which is connected to the CPU (WU, Fig. 3) Thus, the CPU, the graphics controller and the common memory are

synchronized to pass data and address information therebetween with a common clock signal.

As discussed above, Persaud appears to teach a system and method for accessing a common dedicated memory by a plurality of processors. A master processor generates synchronizing signals which are applied over a backplane to each of the slave processors. Handshaking between the master and slave processors is used to control which processor obtains access to an entire particular slave's dedicated memory at any point in time.

Wu's multiple processors utilize a common clock signal and, therefore, would not even contemplate the advantages of using a clock signal representation of a first agent's clock signal, as claimed by claims 1-8, 10-12, 20-21 and 23.

Persaud teaches a system for providing master processor access to a slave processor's dedicated memory. Persaud's master processor and slave processor alternately access the entire dedicated slave processor's memory. Persaud fails to contemplate the need by either of the master processor or slave processor to access a either a partition or portion of an external non-dedicated memory, as claimed by claims 1-8, 10-12, 20-21 and 23.

Neither Wu nor Persaud, either alone or in combination teach access of either portions or partitions of an external non-dedicated memory through a clock representation of a first agent's clock signal, as claimed by claims 1-8, 10-12, 20-21 and 23.

Accordingly, for at least all the above reasons, claims 1-8, 10-12, 20-21 and 23 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claims 14, 15, 17-19 and 22 over Persaud in view of Hughes

In the Office Action, claims 14, 15, 17-19 and 22 were rejected under 35 U.S.C. §103(a) as allegedly being obvious over Persaud in view of Hughes, U.S. Patent No. 5,6784,582 ("Hughes"). The Applicants respectfully traverse the rejection.

Claims 14-15 are dependent on claim 13 and are patentable for the same reasons claim 13 is patentable.

Claims 14, 15, 17-19 and 22 recite, *inter alia*, access of either portions or partitions of an external non-dedicated memory.

As discussed above, Persaud appears to teach a system and method for accessing a common dedicated memory by a plurality of processors. A master processor generates synchronizing signals which are applied over a backplane to each of the slave processors. Handshaking between the master and slave processors is used to control which processor obtains access to an entire particular slave's dedicated memory at any point in time.

Hughes appears to disclose an arbiter for controlling access to an entire shared synchronous memory by a processor complex, a refresh unit, an internal bus, and a core bus (See Hughes, col. 4, lines 1-29; Figure 2). The access requests to the SDRAM are based on size, location, and direction of the transfer (Hughes, col. 6, lines 39-57). Hughes' processor complex provides a memory clock signal in addition to memory access request information (See Hughes, col. 4, lines 49-58). This memory clock signal is the only clock signal provided to shared memory (See Hughes, col. 4, lines 55-58; Figure 2). Other users of the shared memory (the refresh unit, internal bus, and core bus) provide only memory access request information, i.e., starting address, size, and a direction (See Hughes, col. 5, lines 35-45). The other users of the shared memory do not provide any clock signal to shared memory (See Hughes, Figures 2 and 3).

Hughes' arbitration scheme and Persaud's master-slave access both access the entire associated memory. Hughes and Peraud fail to teach access of either portions or partitions of an external non-dedicated memory, as claimed by claims 14, 15, 17-19 and 22.

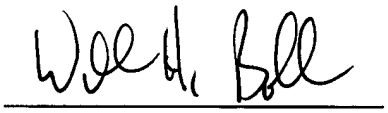
Accordingly, for at least all the above reasons, claims 14, 15, 17-19 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

For at least all the above reasons, claims 1-8, and 10-23 are patentable over the prior art of record.

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



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